1588v2 SLTC IP-Core

Prepare legacy products for PTP 1588v2 Ethernet networks

VeryLogic GmbH
FPGA solutions for Embedded World

General description

The 1588v2 SLTC IP-Core is a Stateless Transparent Clock (SLTC) implementation according to the IEEE 1588v2 standard featuring Precisions Time Protocol (PTP). It is perfectly suited to embed any (legacy) network components (e.g. switches) or IP-Cores and prepare them for synchronized peer-to-peer (P2P) Ethernet networks. The 1588v2 SLTC IP-Core performs all needed peer delay measurements and time (residence time, peer delay and path asymmetry) corrections on behalf of the embedded network component.

Key features

- Unlimited port scalability,
- No configuration required,
- No changes of enclosed component,
- Handling of 1588v2 protocol in HW,
- Low-latency (cut-through) operation,
- One-step operation for redundant networks,
- High accuracy corrections (better than 25 ns),
- Triple (10/100/1000Mbit) link speed,
- (R)(G)MII and reverse PHY interface styles,
- Avalon and AXI-Lite interfaces for SoCs,
- Evaluation kit available,
- Small resource footprint:

Target technology	Resource usage*
Altera Cyclone V	1k ALMs, 3 RAMs
Altera Cyclone IV	4k LEs, 3 RAMs

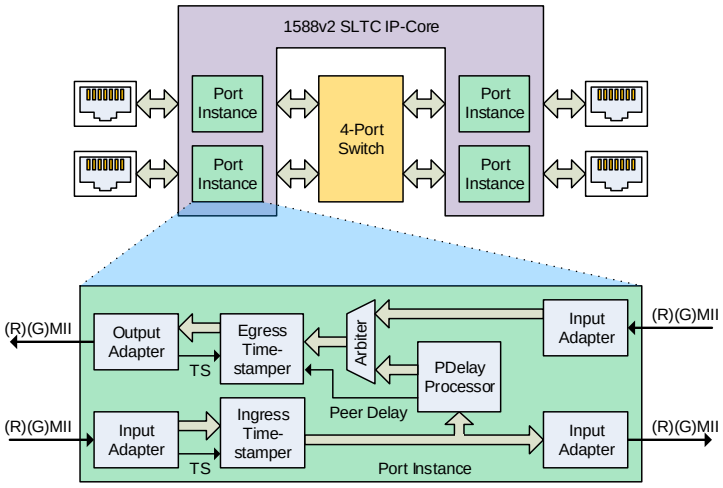
*per port instance

Applications

- Industrial networks,
- Substation automation,
- Defence and Aerospace.

Application example

- PTP-retrofit of a 4-port switch:



Deliverables

- Technology-independent VHDL source code,
- Reference designs for Altera and Xilinx IDEs,
- User testbench and simulation scripts,
- Comprehensive documentation,
- SDC timing constraints.

Related products

- HSR/PRP/1588v2 IP-Core,
- Universal (R)(G)MII Adapter IP-Core,
- Simple Switch IP-Core.

Company profile and contact

VeryLogic GmbH offers FPGA-related design services, especially IP-Core development and verification. For further questions about the products and services, contact us at contact@verylogic.de