PTP Measurements

White Paper

0 Abbreviations

BC	Boundary Clock
DAC	Doubly Attached Clock
FPGA	Field Programmable Gate Array
HSR	High-availability Seamless Redundancy
IEEE	Institute of Electrical and Electronics Engineers
IP	Intellectual Property
IEC	International Electrotechnical Commission
L2	(Ethernet) Layer 2
OC	Ordinary Clock
PDV	Packet Delay Variation
PRP	Parallel Redundancy Protocol
PDelay	Peer Delay
P2P	Peer-to-peer
PHY	Physical layer device
PTP	Precision Time Protocol (also known as IEEE 1588 Std.)
PPS	Pulse Per Second
TCXO	Temperature Compensated Crystal Oscillator
TC	Transparent Clock

1 Introduction

Many industrial applications require precisely synchronized devices gathering process data and exchanging it over Ethernet networks. The IEEE 1588v2 Precision Time Protocol (PTP) is suitable to achieve nanosecond synchronization accuracy between nodes in asynchronous Ethernet networks. This document provides an overview of methodology and measurements used to characterize the hardware-only (software stack is needed only for management messages handling) PTP IP-Cores targeting FPGA-centric embedded systems. The quantitative data shows exceptional performance of the Ordinary Clock (OC) and Transparent Clock (TC) implementations even in high load Ethernet networks. The available accuracy and precision budgets exceed the overall functional requirements of the e.g. smart grid applications by an order of magnitude in the tested situations.

2 Measurements

2.1 Background

Most PTP clocks feature Pulse-Per-Second (PPS) output, which is set at every second boundary for tens of milliseconds. Thus, the relative synchronization error between two clocks can be observed as the delta time between the rising edge transitions of their PPS outputs. During the measurements the positive or negative time delta of the Slave Clock (SC) PPS output transition relatively to the Master Clock (MC) PPS output transition were recorded over a 12 hour period. The recorded delta values are stored in a histogram (Figure 1), which is mathematically processed by the oscilloscope to achieve clock accuracy (= Mean) and clock precision (= 3*Standard Deviation).

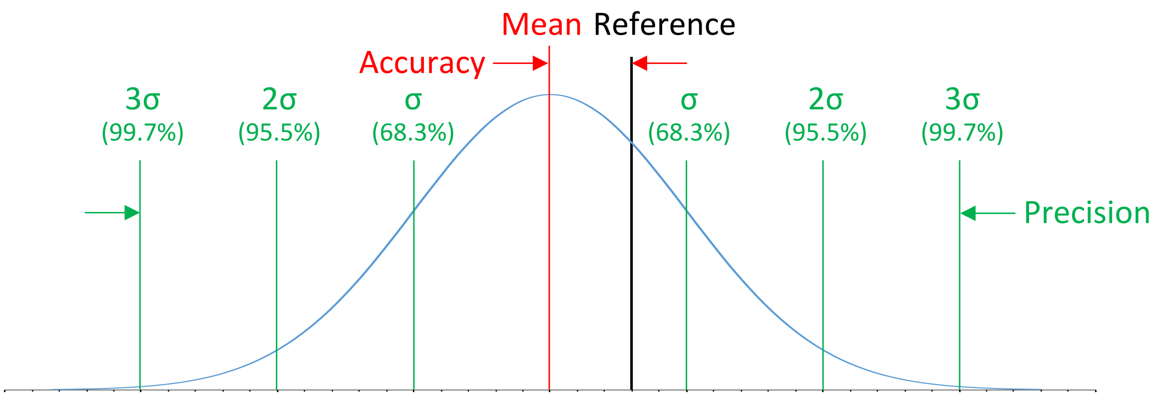

Figure 1: PTP Clock parameters definitions

2.2 Hardware setup

The measurements were executed with the HSR/PRP/PTP-Core and OC-Core instantiated at the DemoBox platform (Figure 2). The HSR/PRP/PTP-Core features Redundant Ethernet, Doubly Attached Clock (DAC, which is redundant combination of two OCs) and Transparent Clock functionality according to IEC 62439-3.4/5 and IEEE 1588v2 Standards. The OC-Core combines Ordinary and Transparent Clock implementation according to IEEE 1588v2 Standard, which is extendable to Boundary Clock (BC) with an additional software stack. The IP-Cores are highly customizable and handle the synchronization-related PTP messages purely in hardware. This avoids software overhead and related timing issues by design.

Figure 2: Cascaded TC measurement setup

The key parameters for all performed measurements were:

- IEEE 1588v2 peer delay Layer 2 protocol (L2P2P),
- One Sync and PDelay message per second rate,
- One Announce message per 2 seconds rate,
- Asynchronous Gigabit link speed with 15cm LAN cables,
- Low-Cost TCXOs both in Ordinary and Transparent Clocks.

The oscilloscope measurements interpretation is explained in Figure 3 and Table 1.

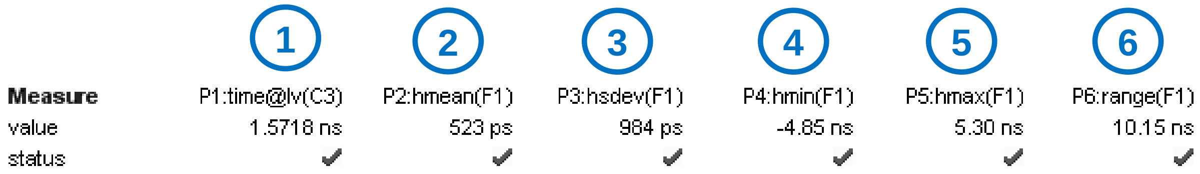

Figure 3: Oscilloscope measurement readout

Nr.	Measurement	Interpretation
1	time@lv	Time delta at a predefined level (0.75V for all measurements) between last MC PPS1 and SC PPS1 transitions. The value is also shown graphically.
2	hmean	Histogram mean = clock accuracy.
3	hsdev	Histogram Standard Deviation. Clock precision equals 3*Standard Deviation.
4	hmin	Histogram minimum. Horizontal position of the most left SC PPS1 transition.
5	hmax	Histogram maximum. Horizontal position of the most right SC PPS1 transition.
6	range	Horizontal range of all SC PPS1 transitions. The range is also shown graphically.

Table 1: Oscilloscope measurement interpretation

2.3 Directly Connected Clocks

The direct connection of the Master Clock (MC) and Slave Clock (SC) (Figure 4) eliminates the potential negative effect of Packed Delay Variation (PDV) and related residual time correction errors introduced by the Ethernet switches with integrated TCs. However, this ideal setup has limited practical relevance; at the same time, it provides measurement results widely used in industry to compare different commercially available PTP OC implementations.

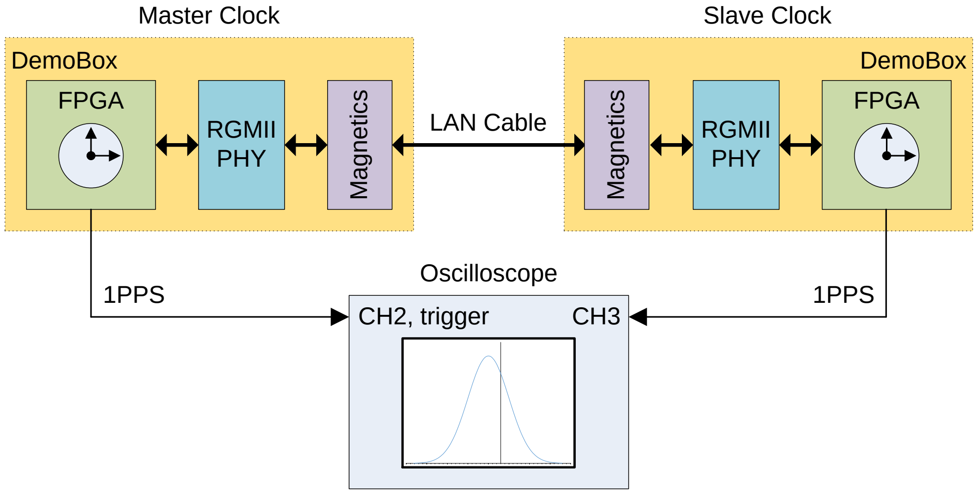

Figure 4: Directly connected Master and Slave Clocks test setup

Clock accuracy of ca. 0.5 ns (hmean) and clock precision of ca. ±3 ns (3*hsdev) were achieved (Figure 5). All SC PPS1 transitions lay within ca. ±5 ns range around the MC PPS1 reference signal. Faster Sync message rate of two messages/sec. results in negligible improvements, therefore the related measurement diagrams are omitted.

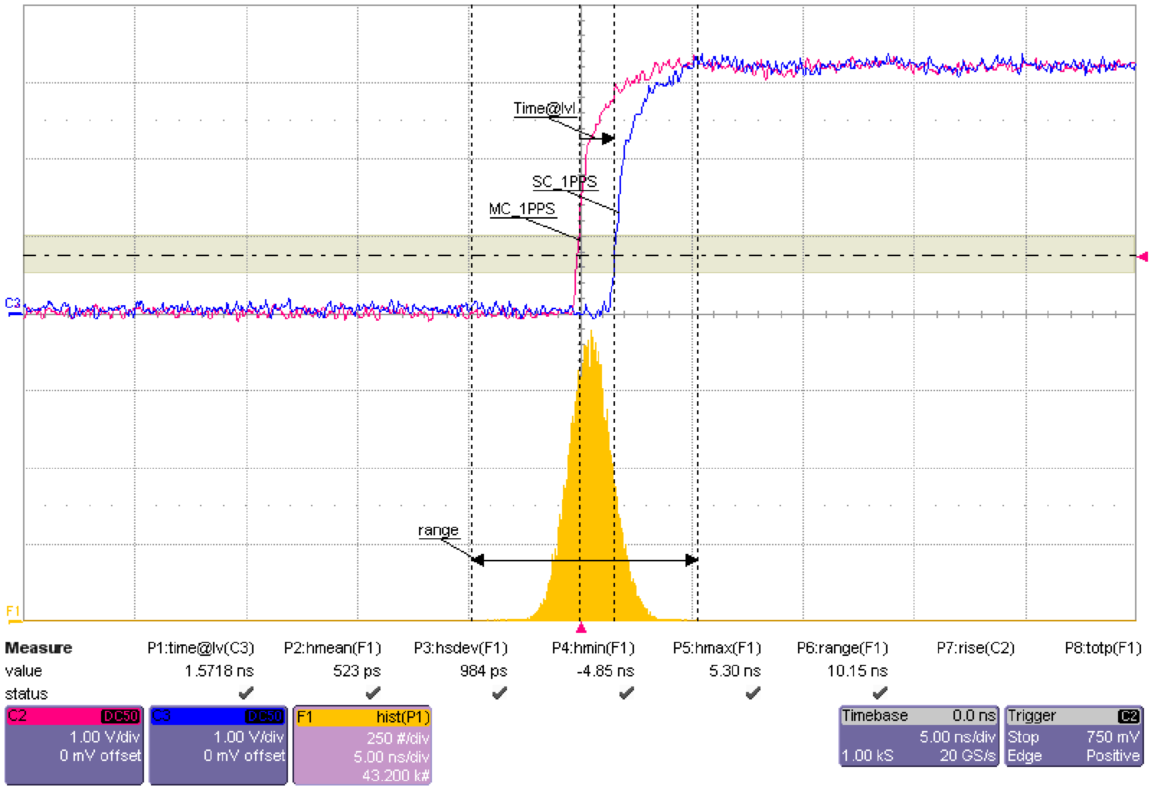

Figure 5: Directly connected clocks measurement

2.4 Single Transparent Clock

The influence of a Transparent Clock (TC) on time synchronization was assessed by placing a single TC between master and slave clocks (Figure 6).

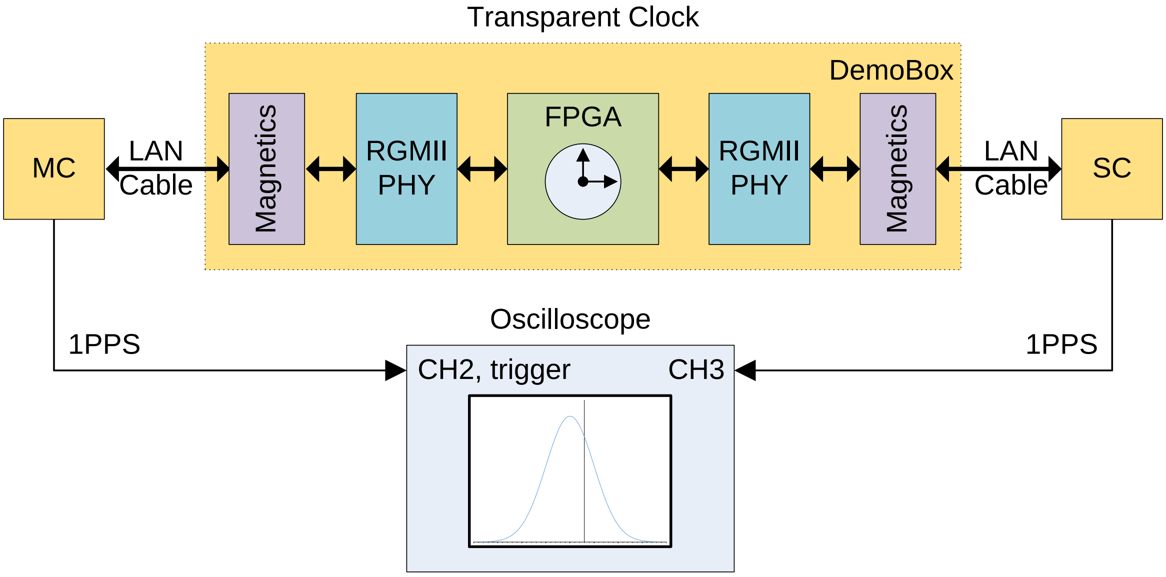

Figure 6: Single Transparent Clock test setup

Clock accuracy of ca. 1.1 ns (hmean) and clock precision of ca. ±6 ns (3*hsdev) were achieved (Figure 7). All SC PPS1 transitions lay within ca. ±10 ns range around the MC PPS1 reference signal. In other words, a single TC deteriorates the measured parameters by nearly factor two.

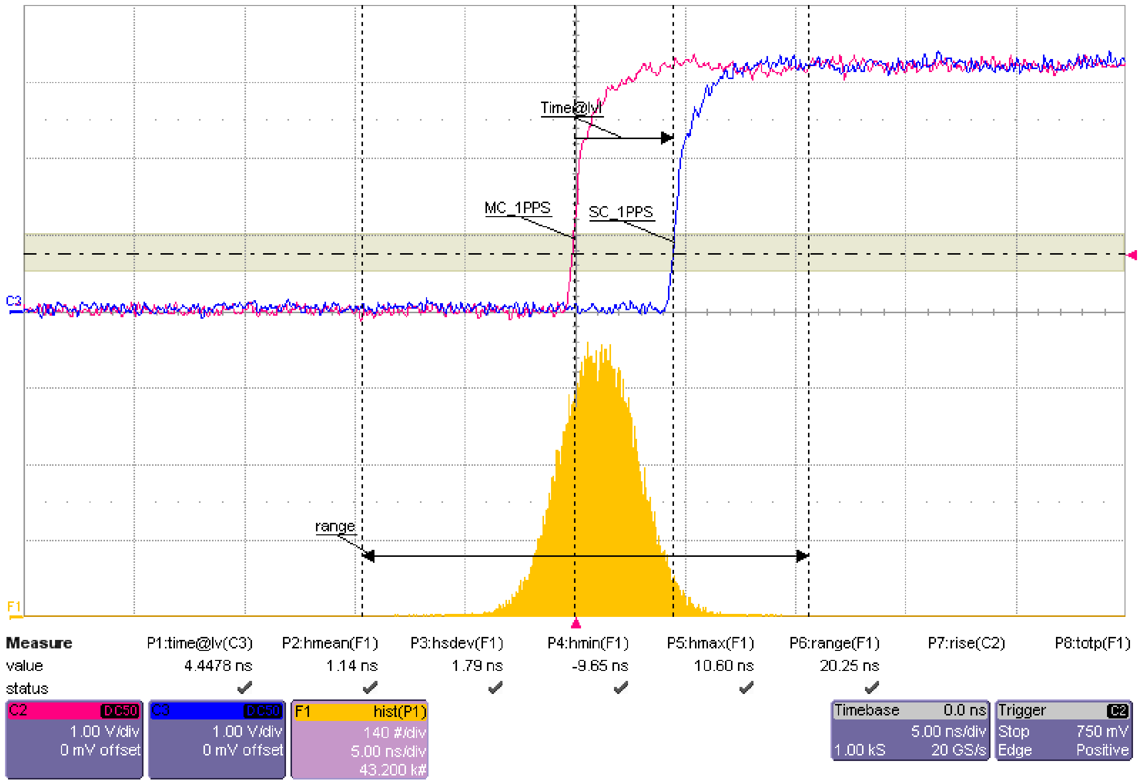

Figure 7: Single Transparent Clock measurement

2.5 Cascaded Transparent Clocks

The influence of multiple Transparent Clocks on time synchronization was assessed by placing 15 TCs between master and slave clocks according to IEEE Std. C37.238 (Figure 8). An additional slave clock is placed after 9 TCs for comparison. Each of the first 8 TCs can be connected to the optional 100 Mbit Traffic Generators, which inject 800 Mbit broadcast frames with equally distributed lengths into the TC chain.

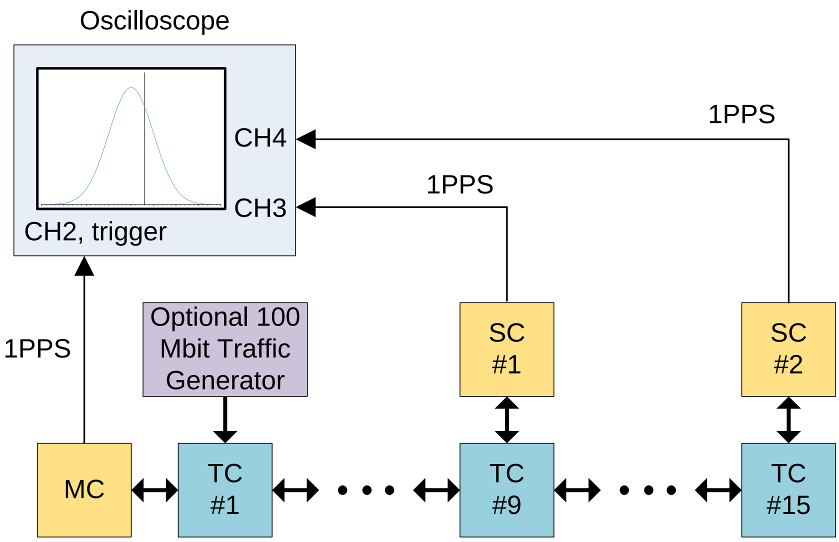

Figure 8: Cascaded Transparent Clocks test setup

The first reference test was performed without network traffic (Figure 9). Clock accuracy of ca. 10 ns (respectively 8 ns) and clock precision of ca. ±25 ns (respectively ±20ns) were achieved after 15 TCs (respectively 9 TCs, yellow histogram). All SC #1 PPS1 transitions lay within ca. ±40 ns range around the MC PPS1 reference signal. All SC #2 PPS1 transitions lay within ca. ±50 ns range around the MC PPS1 reference signal.

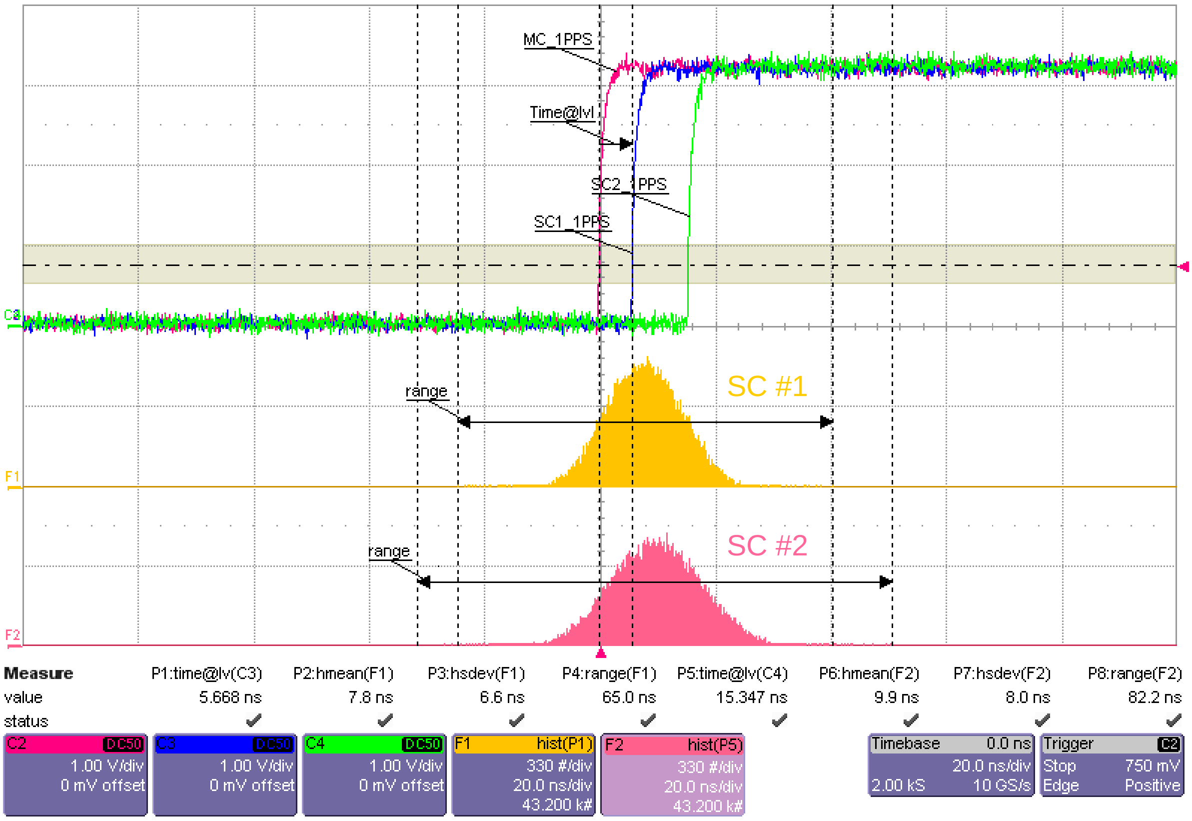

Figure 9: Cascaded TC measurement without traffic

Hence the TCs operate in cut-through mode, the propagation delay introduced by the whole TC chain to the Sync messages is just around 22.8 µs (Figure 10) at no network traffic condition. TCs measure and update the residence time and path delay in the Correction Field of Sync messages, which equals to the total delay.

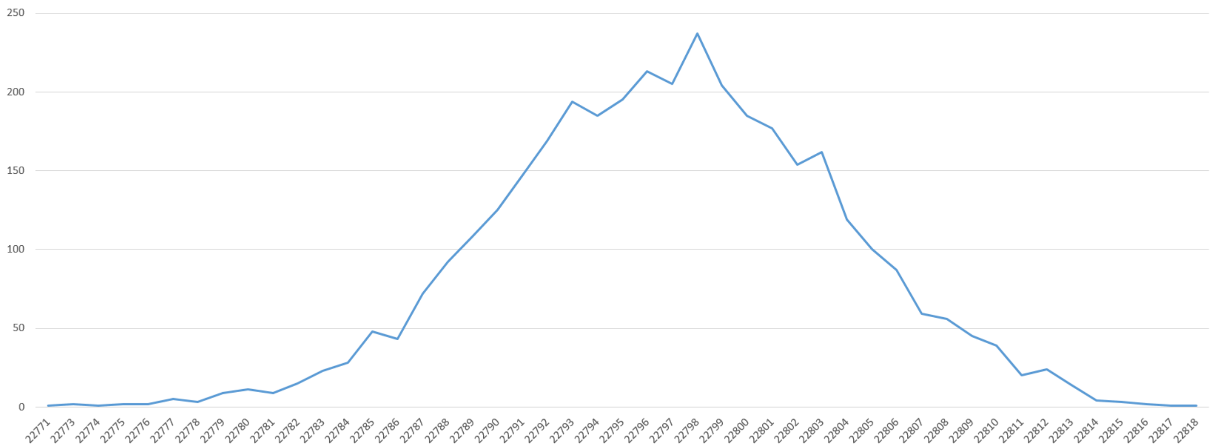

Figure 10: Correction Field value distribution of 3,600 Sync messages

The second test was performed with 80% respectively 800 Mbit network load. The frames injected by the Traffic Generators introduce additional delay to the Sync frames. After 1 hour Correction Field recording, a maximum total delay of ca. 84µs was observed once (Figure 11).

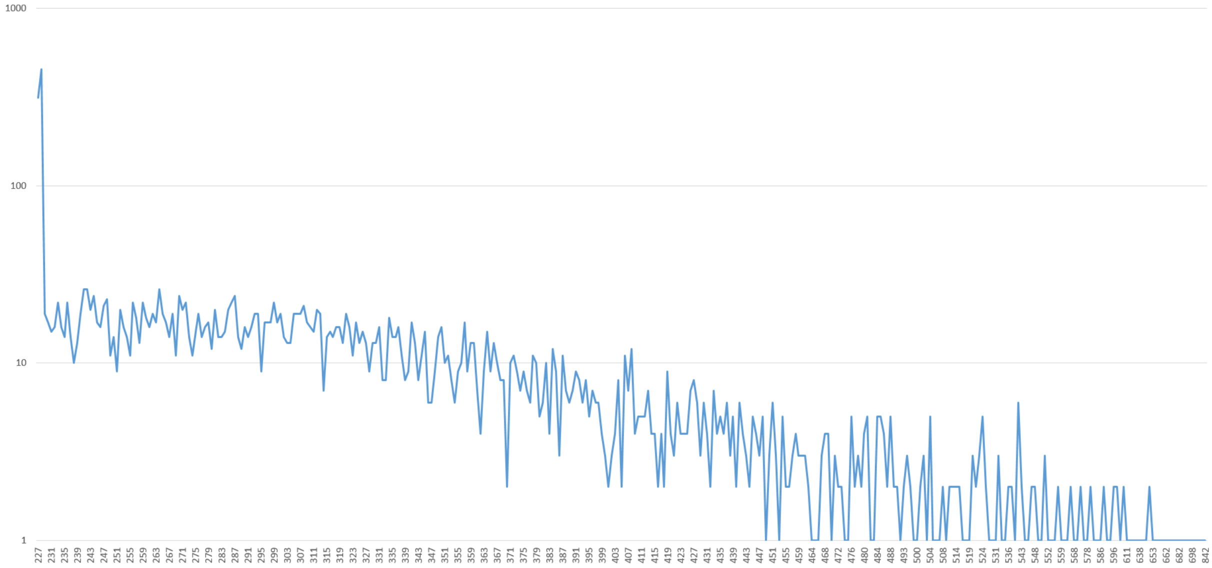

Figure 11: Correction field value distribution of 3,600 Sync messages with 80% additional network traffic

No deterioration of clock accuracy and precision was measured with the additional network traffic. As expected, the additional traffic caused only negligible measurement variation (Figure 12).

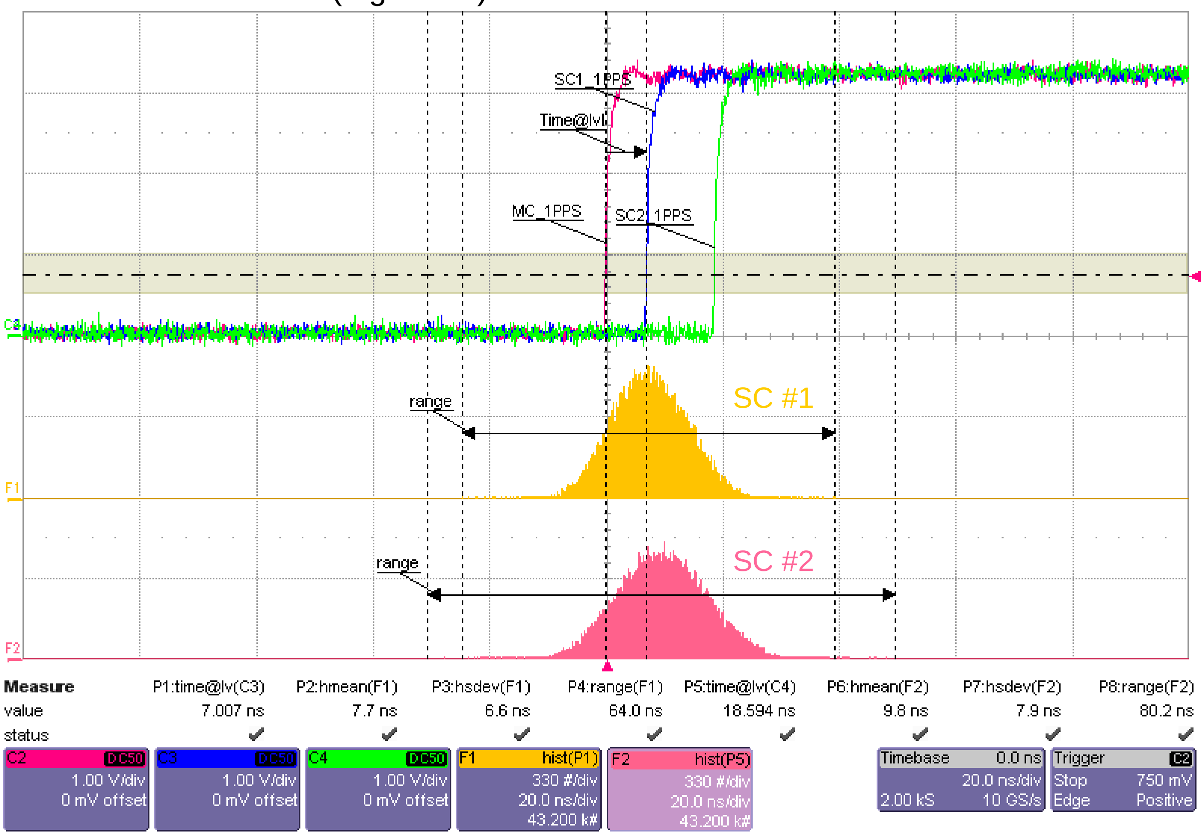

Figure 12: One Sync message per second measurement without traffic

3 Summary

The measurements demonstrated exceptional performance of the hardware-only implementation of the Ordinary and Transparent Clock IP-Cores. Even with the low-cost TCXO the delivered performance was more than one order of magnitude better than the IEEE Std. C37.238 clock accuracy and precision requirements. Due to Ordinary Clock servo robustness the message rates higher than one Sync message per second are no longer required to fulfil the current automation applications requirements. With a precise Transparent Clock residence time correction the user doesn’t need to be concerned of the Sync message Packet Delay Variations. In fact, with the demonstrated solution the network traffic no longer plays any role in the L2P2P time synchronization networks.

4 Appendix

4.1 Document history

Version	Date	Author	Comment
1.0.000	2017-04-30	VM	Initial version