PRP-Core user manual

(web edition)

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0 Abbreviations

DAN	Dual Attached Node
DDR	Double Data Rate
DMAC	Destination MAC
EthType	Ethernet Type
FCS	Frame Check Sequence
FIFO	First In First Out
FPGA	Field Programmable Gate Array
HAL	Hardware Abstraction Layer
ID	Identifier
IEC	International Electrotechnical Commission
IO	Input Output
IP	Intellectual Property
LAN	Local Area Network
LE	Logic Entity
LRE	Link Redundancy Entity
LSDU	Link Service Data Unit
MAC	Media Access Control (or Controller)
µCU	Microcontroller Unit
NDA	Non-Disclosure Agreement
P&R	Place and Route
PCB	Printed Circuit Board
PHY	Physical layer device
PLL	Phase Locked Loop
PRP	Parallel Redundancy Protocol
RCT	Redundancy Check (or Control) Trailer
RedBox	Redundancy Box
REG	Register
RGMII	Reduced Gigabit Media Independent Interface
SAN	Singly Attached Node
SANA	SAN connected to LAN A sub-network
SANB	SAN connected to LAN B sub-network
SeqNr	Sequence Number
SMAC	Source MAC
SMI	Serial Management Interface
SNMP	Simple Network Management Protocol
(S)RAM	(Static) Random-Access Memory
TCP/IP	Transmission Control Protocol/Internet Protocol
VDAN	Virtual DAN (SAN connected to a PRP network through a RedBox)
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VLAN	Virtual LAN

1 Introduction

1.1 Summary

The PRP-Core is a Link Redundancy Entity (LRE) implementation according to the IEC 62439-3.4:2011 standard subset dedicated to PRP and can be used for both DAN and RedBox designs. The PRP-Core is suitable for the 10/100/1000 MBit Ethernet networks. It is the standard-closest implementation with the smallest FPGA resource footprint available (the full-featured PRP-Core fits in a 5$ low-cost FPGA[1]). Table 1 gives an overview of the PRP-Core feature set and its implementation details. A free hardware evaluation kit (DemoBox) is available on request.

Feature	Implementation details
Duplicate accept and discard modes	Duplicate discard is based on linear search algorithm, with up to 4096[2] table entries. Configurable[3] Entry Forget Time.
VLAN support	Optional[3] frame filtering is based on configurable VLAN ID.
Monitoring Data Set	Provides basic network health status information.
Frame size	Restricted by RCT LSDU field width to max. 4096[2] bytes.
Frame FIFO size	Frame FIFO size[2] is only limited by the target FPGA block RAM resources.
Link speed	10/100/1000 MBit link speeds are supported on all ports. Link speed and link status are monitored.
Physical Interface	RGMII. Hardware Abstraction Layer (HAL) provided to adapt to different physical interfaces (e.g. MII, RMII, GMII).
MAC Table	Frame filtering is based on the MAC addresses of the up to 16 served SANs connected to non-redundant network.
Nodes Table	Optional[2] hardware-only (no software stack is required) implementation with up to 256 node entries. Configurable[3] Node Forget Time.
Network Supervision	PRP-tagged Supervision frames are generated[3] for every SAN connected to the non-redundant network. Supervision frames are handled inside the PRP-Core and are optionally[3] forwarded to the non-redundant network.
Network Management Interface via TCP/IP SNMP	No direct support. If needed, should be implemented in a Local Application. For this purpose the health status of the PRP network is collected in Monitoring Data Set and Nodes Table accessible via Register Set.
Bridging mode	Optional frame forwarding between LAN A/B is not supported.
Target technology	SRAM-based low-cost FPGAs (e.g. Altera Cyclone IV or Xilinx Spartan 6). Technology independent VHDL implementation.

Table 1: PRP-Core implementation details

[1]**Note:** Volume price of the Altera EP4CE10 FPGA with 10k logic entities

[2]**Note:** Configurable at source code level

[3]**Note:** Configurable via Register Set

1.2 Theory of operation

The Parallel Redundancy Protocol (PRP) provides zero-switchover time in case of a fault by the duplication of both network infrastructure and frames sent to the network (Figure 1). A PRP network consists of two independent Local Area Networks (LAN A respective LAN B) of similar topology and thus of similar frame delay times. The connection of a communication node to the RPR network is done through the Link Redundancy Entity (LRE), which is a software stack or hardware implementation (e.g. FPGA) inside the node (Figure 2). The LRE is responsible for creation duplicates of outgoing frames and removing duplicates of the incoming frames. Hence the communication is fully transparent for higher level protocols and applications.

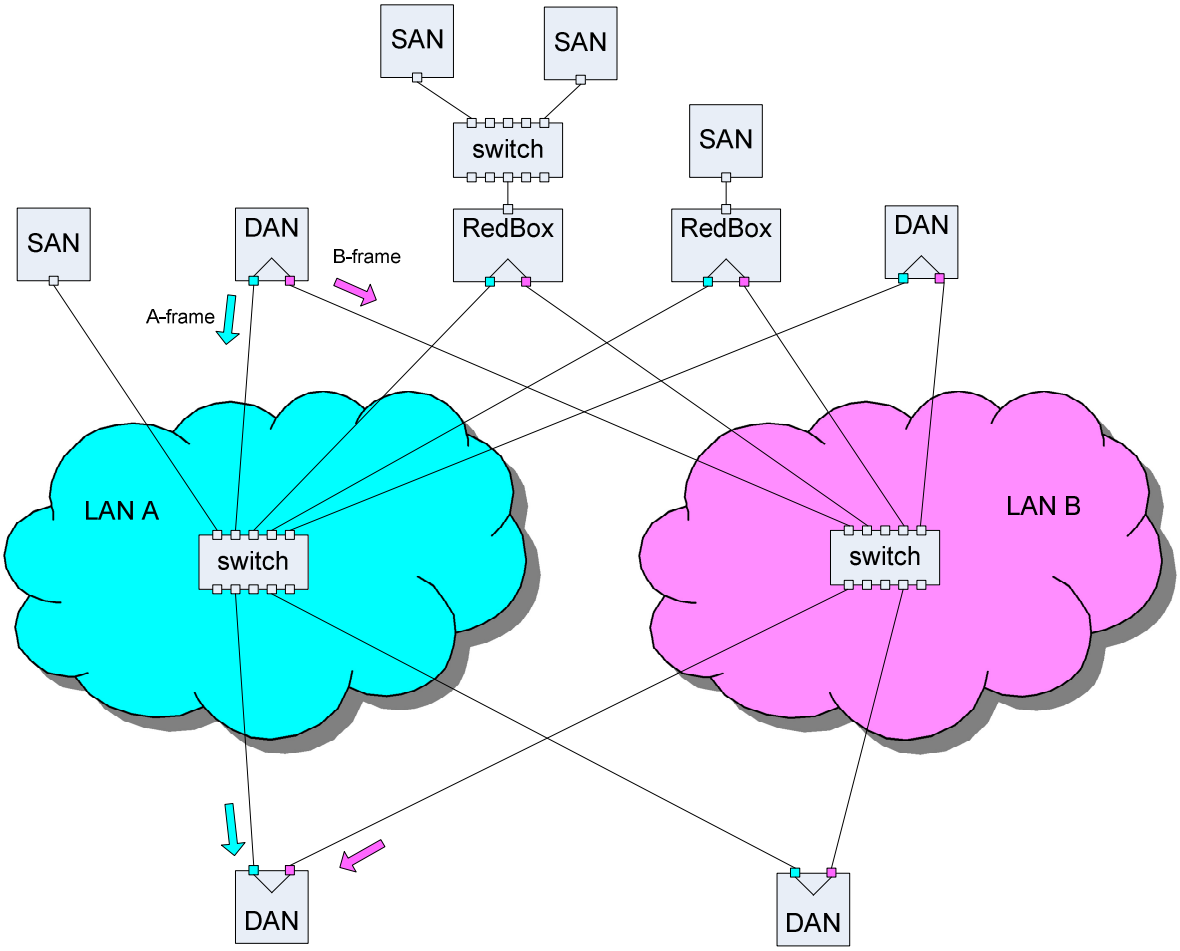


Figure 1: PRP network example

Nodes connected to both LAN A and LAN B through a LRE are called Dual Attached Nodes (DANs). Nodes, which communication is non-critical (e.g. printers) can be connected directly to one of the both PRP sub-networks. These nodes are called Singly Attached Nodes (SANs) and they can communicate with all DANs but only with SANs in the same sub-network (LAN A or LAN B). A SAN connected through a Redundancy Box (or RedBox for short, which is a LRE implementation in a separate device, Figure 3) to the PRP network appears as a DAN to all other nodes and is called Virtual DAN (VDAN). A RedBox can connect more than one SAN to the PRP network. Only DANs and RedBoxes support redundancy in a PRP network.

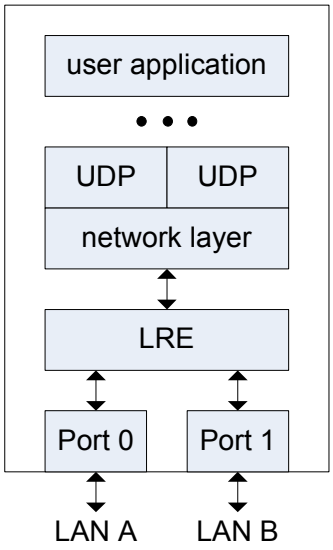


Figure 2: Principal DAN structure

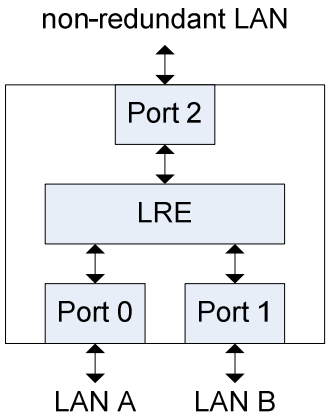


Figure 3: Principal RedBox structure

During the transmission a frame received from upper network layers is duplicated by the LRE and Redundancy Check Trailers (RCTs) are added to the duplicates at the frame end. The adding of a RCT to a frame is also called tagging. A RCT contains additional information, which allows detection and thus rejection of the frame duplicates at the destination node. When the first frame arrives at the destination node, the RCT is removed from the frame by the LRE and the original frame content is passed to the node. The RCT and Source MAC (SMAC) of the received frame are stored in the Entry Table which is a mandatory part of a LRE. The RCT and SMAC of every received frame are compared to all valid entries in the Entry Table. If an entry with same RCT and SMAC is already present in the Entry Table, then the received frame is a duplicate and thus it's rejected. The entries in the Entry Table are removed (aged out) after elapsing of the Entry Forget Time since their creation.

The frames originated by a SAN are not handled by a LRE and thus a SAN doesn't support redundancy. Because a SAN operates only in one LAN, it receives only the frames sent by a DAN to this specific sub-network, thus no duplicate rejection is needed. A RCT added by a LRE to the outgoing frame is ignored by a SAN due to inherent tolerance of the upper level network protocols to the RCT at the frame end.

An untagged Ethernet frame consists of Destination MAC (DMAC), Source MAC (SMAC), Ethernet Type of the supported protocol (EthType), payload and Frame Check Sequence (FCS). During the frame tagging in the LRE a RCT is added between the payload and FCS. The RCT consists of Sequence Number (SeqNr), LAN Identifier (LAN ID), Link Service Data Unit (LDSU) and PRP suffix which is always 0x88FB hexadecimal (Figure 4). The Sequence Number represents the value of a 16 bit counter, which is incremented after every frame duplication and RCT tagging, i.e. the duplicates of a frame have the same Sequence Number. The LAN ID value is 0xA if the frame duplicate is sent to the LAN A and 0xB if the duplicate is sent to the LAN B. The LAN ID is the only field which differs between the duplicates of a frame. Thus, the FCS of frame duplicates is always different. The LSDU represents the length of both frame payload and RCT in bytes. Hence the RCT is placed after the frames payload, it is interpreted as meaningless frame padding by upper network layer protocols in a SAN. This property ensures smooth communication between the DANs and SANs in a PRP network.

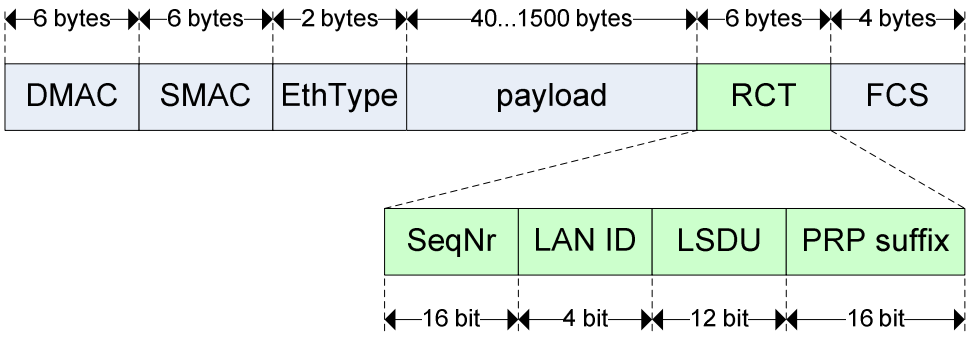


Figure 4: Structure of a PRP-tagged frame

Redundancy helps little, if the network failures can't be detected. Thus the IEC 62439-3.4:2011 standard defines mechanisms, how PRP network health status shall be collected and represented. Each frame received by a LRE is used to update the standard-defined Monitoring Data Set and the optional Nodes Table. The Monitoring Data Set consists of several data objects, which can be read by the user application:

- **SendSeq**: Represents the value of the 16-bit counter used in the local LRE for SeqNr generation and thus for tagging of the outgoing frames.
- **CntErrA/B**: Number of erroneous frames (e.g. with wrong FCS) received over LAN A respective LAN B.
- **CntReceivedA/B**: Number of frames received over LAN A respective LAN B.
- **CntErrWrongLanA/B**: Number of frames received with wrong LAN ID over LAN A respective LAN B.
- **ActiveA/B**: Represents communication link status.

In contrast to the Monitoring Data Set, the optional Nodes Table provides more detailed network status information. Each entry in the Nodes Table reflects status of a specific node in the PRP network:

- **MacAddress**: MAC address of the node.
- **CntReceivedA/B**: Number of frames received from that node over LAN A respective LAN B.
- **CntErrWrongLanA/B**: Number of frames received from that node with wrong LAN ID over LAN A respective LAN B. These objects reveal nodes wrongly connected to the PRP network.
- **TimeLastSeenA/B**: Time at which the last frame was received from that node over LAN A respective LAN B. Can be used to detect communication link loss.
- **SanA/B**: True, if that node is accessible over LAN A respective LAN B. If both objects are true, than that node is a DAN, otherwise it's a SAN.

An entry is removed from the Nodes Table if no frames were received from the according node over PRP network for a time period longer than the Node Forget Time. Hence the upper level protocols can't be expected to send frames periodically in order to prevent aging out of the Nodes Table entries, Supervision frames are generated automatically by the LRE every two seconds. They do not only refresh the

TimeLastSeenA/B objects but also provide additional information about the source node (e.g. whether the source node rejects or accepts duplicates).

1.3 Functional description

1.3.1 PRP receive path

The PRP-Core contains the whole LRE functionality. In the receive path frames coming from the LAN A or LAN B of the PRP network are first converted by Input Adapter from RGMII to PRP-Core internal byte-oriented bus running at 250 MHz. The incoming frames are directly stored in the Receive FIFOs (Figure 5).

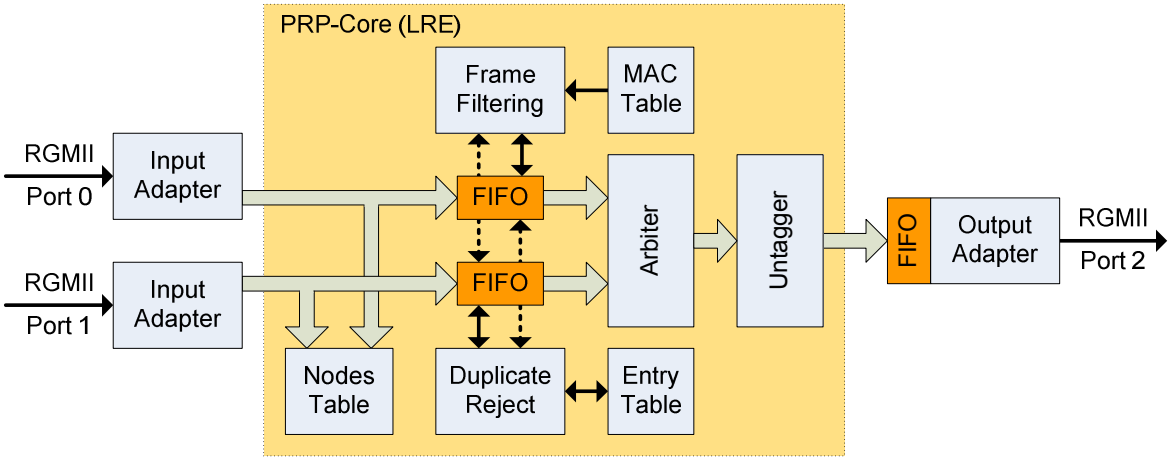


Figure 5: PRP-Core receive path block diagram

During the frame reception and storage, a decision is made by Frame Filtering and Duplicate Reject components, whether to store the incoming frame or to drop it. The frame is dropped if one of the following rules applies:

- Frames FCS is invalid,
- Frame was received on the correct path (LAN A for port 0 and LAN B for port 1) and a valid entry with the same Sequence Number and SMAC address was found in the Entry Table,
- VLAN-based frame filtering is enabled and the VLAN-tagged frame has a different VLAN ID than specified in the Register Set,
- Frames DMAC address was not found in the MAC Table,
- Frame is a PRP Supervision frame and Supervision frame forwarding to non-redundant network is disabled in the Register Set,
- Frames size exceeds free memory size in the Receive FIFO.

If a frame was dropped, then the storage memory it allocates in one of the Receive FIFOs is immediately freed. Dropping the frames in this way prevents wasting costly FPGA memory resources, because only the frames to be forwarded to non-redundant network are stored in the both Receive FIFOs.

If the frame wasn't dropped and contains a valid RCT then a new entry is created in the Entry Table with the current timestamp. An entry is deleted when Entry Forget Time elapses since its creation. The frames stored in Receive FIFOs are forwarded to the Outputs Adapter FIFO for the transmission to the non-redundant network. The

Output Adapter performs visa-versa conversion of PRP-Core internal byte-oriented bus to the RGMII. The Untagger in the front of the Output Adapter removes detected RCTs from the outgoing frames.

The PRP-Core features optional Nodes Table as specified in IEC 62439-3.4:2011 standard. The usage of the Nodes Table can be enabled at the source level. In contrast to commercially available FPGA IP-cores, a full fledged, hardware only (without the need of software stack) solution is provided. The existing software stack based solutions silently ignore standard requirement of processing *all frames* received over both LAN A *and* LAN B. They can't and don't process duplicates, because duplicates are already rejected in the LRE and thus not forwarded to non-redundant port for further processing.

The implemented Nodes Table receives and processes all incoming frames. If VLAN feature is enabled, only the frames with the same VLAN ID are processed. The readout of the Nodes Table entries is done via Register Set, which can be connected to a microcontroller unit (µCU). Up to 256 entries are supported. The linear search of the whole Nodes Table for the next valid entry would cause a noticeable µCU processing time overhead. Thus the search algorithm is implemented in PRP-Core. The search of the next valid entry is started by setting the Nodes Table Read Request (NREQ) bit in CCTRL2 register. When the next valid node entry was found in the Nodes Table and it was copied to Register Set for readout, the NREQ bit is cleared and an interrupt event is generated to signal available data. The user is strongly encouraged not to poll NREQ bit in order to detect the end of search process, but to use the interrupt functionality hence the search time is not deterministic and may consume several microseconds.

1.3.2 PRP transmit path

When a frame is received from non-redundant network, its SMAC is learned by the MAC Table. The incoming frame is stored in the Tagger FIFO first. After full reception with subsequent PRP tagging the duplicated and tagged frames are forwarded to the Port 0/1 Output Adapters FIFOs (Figure 6).

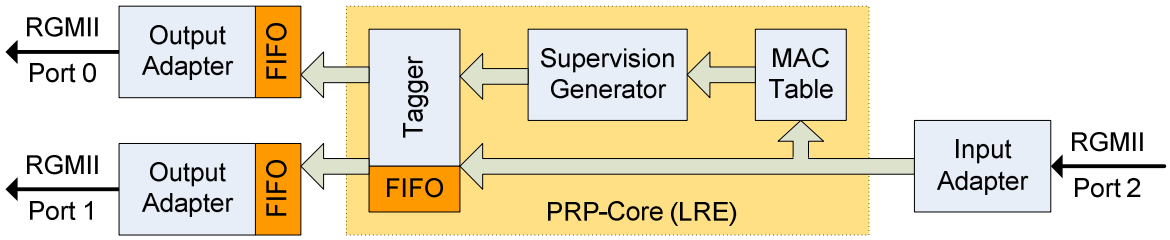


Figure 6: PRP-Core transmit path block diagram

The duplicated frames are always forwarded to redundant network with the maximum link speed detected either on Port 0 or Port 1. Thus the FIFO size in the Tagger needs to be slightly larger than maximum frame size (i.e. 2 kByte Tagger FIFO size for 1518 byte frame are sufficient). For the same reason the Output Adapters FIFOs can be set to a minimum size of 1 kByte. If one of the Output Adapters operates at slower link speed than the other (e.g. 100 MBit instead of 1000 MBit), then its frames are lost because they are sent with higher speed (remember, maximum detected link speed of Port 0 or Port 1 is used for transmission). The other port is transmitting frames with correct (higher) link speed. This faulty state can be easily detected by the usage of the Nodes Table (the according DAN appears then as SAN) or by

observation of the Link Status field in Link Status Register and shall be fixed by the network administrator. In contrast to existing commercial solutions with unified memory approach (one shared memory for both receive and transmit paths), that faulty state has no impact to the receive path operation. In unified memory approach any incoming frame is dropped, if the shared memory is full, which may be the consequence if one of the ports operates at lower link speed than other ports.

Every two seconds two Supervision frames (one for each sub-network) are generated by Supervision Generator for each node connected to non-redundant network. It uses valid MAC entries in the MAC Table to generate Supervision frames on behalf of the nodes attached to the non-redundant network. To avoid any impacts on the regular frame traffic handled by the Tagger, the Supervision frames are transmitted only when FIFOs in both Output Adapters and in Tagger are empty.

1.3.3 Use cases

The PRP-Core can be used for stand-alone RedBox between a PRP network and up to 16 SANs on a non-redundant network (Figure 7). Stand-alone usage implies that the PRP-Core settings are static (i.e. preconfigured at the source code level) and the health status of the PRP network is not collected in the RedBox. The Supervision frames however are still generated for each SAN.

The managed RedBox use case allows dynamic core configuration and PRP network health status supervision. This requires a µCU (either external or embedded in the FPGA) with a connection to the non-redundant network and to the Register Set of the PRP-Core (Figure 8). Although co-located to RedBox, the µCU is in fact another SAN in the non-redundant network. The optional Network Management Interface via TCP/IP SNMP can be a part of Local Application implementation.

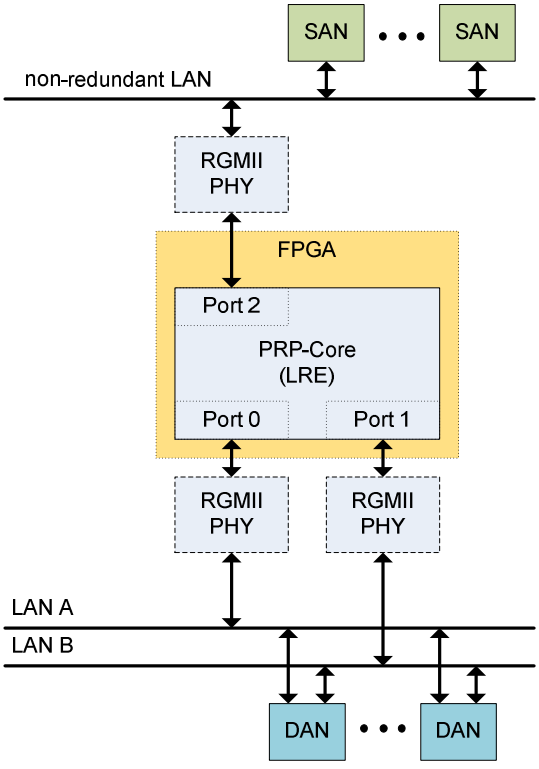


Figure 7: Stand-alone RedBox use case

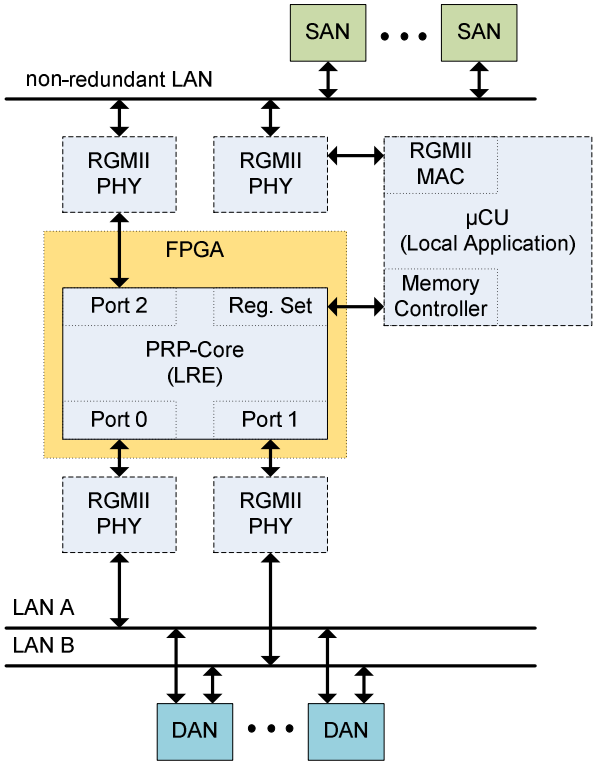


Figure 8: Managed RedBox use case

If only a single device shall be connected to the PRP network, then the DAN use case should be preferred (Figure 9). The µCU (either external or embedded into FPGA) is directly connected to the non-redundant port (Port 2) of the PRP-Core. The DAN use case allows dynamic core configuration and health status supervision of the PRP network. The optional Network Management Interface via TCP/IP SNMP can be a part of Local Application implementation.

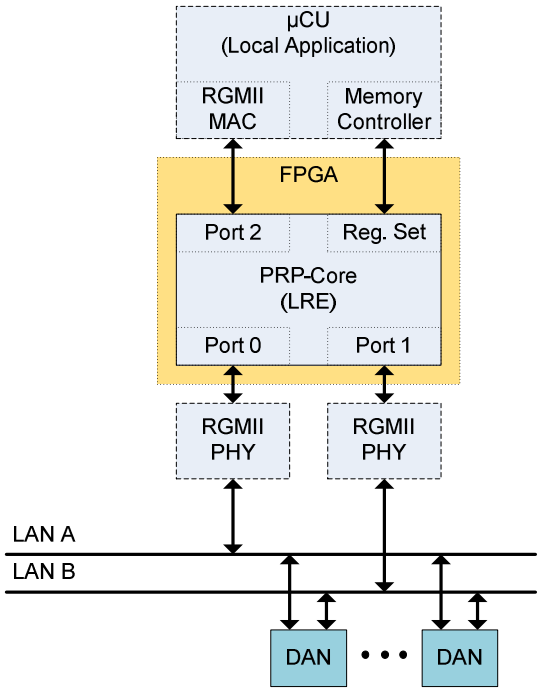


Figure 9: Dual Attached Node (DAN) use case

In high-traffic application the DAN use case should be preferred to the RedBox use cases hence the network traffic through a RedBox is always shared by all SANs connected to the non-redundant network. Thus, a RedBox (independent of manufacturer and implementation) might be a traffic bottle-neck between PRP and non-redundant networks. The small FPGA resource usage of the PRP-Core reduces however DAN and RedBox implementation costs if compared to other PRP implementations currently available.

1.3.4 Standard deviations

There are some deviations from IEC 62439-3.4:2011 standard in the current PRP-Core implementation, which are documented in this section.

First deviation applies to standard requirement, to send non-tagged frames to a SAN only through the sub-network where it's registered, when the Nodes Table is present. In the current PRP-Core implementation there is no connection between Nodes Table and the Tagger component. Thus the Tagger doesn't know whether an incoming frame is sent to a SAN or to a DAN. Even when the communication is done with a SAN, tagged duplicate frames are sent over both Port 0 and Port 1 to LAN A respective LAN B of the PRP network. However the standard notes that such operation mode has only negligible impact to overall network performance and the PRP RCT is naturally tolerated by all SANs. Furthermore, this is the only operation mode of any LRE implementation without (optional) Nodes Table.

According to the standard, the TimeLastSeenA/B attributes shall represent local time at which the latest frame from the according node was received. Hence the PRP-Core doesn't yet support time synchronization and thus local time reference, the meaning of the TimeLastSeenA/B fields deviates from standard specification. It represents the time in seconds since the reception of the latest frame from the according node.

After a reception of Supervision frame the standard requests an update of the DAN Duplicate Accept or Duplicate Reject attributes in the Nodes Table. These fields are not explicitly shown in the "Table 1" in the section "4.2.7.2 Nodes Table" of the standard. However, both fields are contained in the current Nodes Table implementation. In conjunction with SanA/B fields they allow easy detection of DANs with disconnected Port 0 or Port 1.

1.4 Configuration and customization options

The Input/Output Adapters provides a Hardware Abstraction Layer (HAL) from PHY-specific interface protocol to the PRP-Core internal byte-oriented bus and visa-versa. At the moment only RGMII interface style is supported. The specification of the byte-oriented bus is available under NDA condition, afterwards the user is able to create his own Input/Output Adapter implementations for different interface styles and also add his own logic between Input/Output Adapters and the PRP-Core. Alternatively, any interface style Input/Output Adapter can be created on request.

The PRP-Core is highly throughput optimized in order to be able to process frames coming from a 1000 MBit Ethernet network. In fact it can handle bandwidths of 250 MByte/s per port. Therefore the core clock can be reduced to $1/10^{th}$ (25 MHz) of the specified 250 MHz, if the core is used in the 10/100 MBit network only. This reduces the required dynamic power consumed by the core to $1/10^{th}$ and makes timing closure at slowest speed-grade and lowest-power FPGAs possible.

Note: The RGMII Input/Output Adapter must be replaced or redesigned if the PRP-Core clock shall have a different value than 250 MHz.

The PRP-Core can be configured statically at the source level prior synthesis step and dynamically via the Register Set (see section 3 for details). The source level configuration options are:

- Nodes Table usage,
- Entry Table size (up to 4096 entries),
- Maximum frame size (up to 4096 bytes),
- Register Set reset values (for stand-alone use case),
- Receive-, Tagger- and Output Adapter-FIFO sizes.

1.5 Core evaluation and ordering information

A functionally limited RedBox netlist (PRP-Core without Nodes Table) for the Altera Cyclone IV FPGAs is available for core evaluation and non-commercial usage. The registration-free download package includes an Altera Quartus II example design for the Terasic DE2-115 and Ethernet HSMC evaluation boards. For registered industrial users a custom hardware evaluation platform called DemoBox is offered, which features a full-fledged PRP-Core with Register Set monitor software.

The commercial versions of the PRP-Core and of the Input-/OutputAdapter are provided either as a gate netlist for specific FPGA technology or as obfuscated VHDL source code. For the netlist delivery all PRP-Core customization options and generics need to be specified by the customer. The delivery package includes example SDC timing constraints and a simple VHDL testbench which can be used to verify core functionality after Place and Route (P&R) design step. The maintenance updates are provided free of charge. One year of optional technical support is offered separately.

1.6 Interface description

The following section describes external interface of the RedBoxTop top-level component. The RedBoxTop component is the structural description of a RedBox which includes PRP-Core and other components (Figure 10) except Phase Locked Loop (PLL). The generics are only available for the VHDL source code option. Hence they are synthesized away when the netlist is generated, the generics values must be specified beforehand.

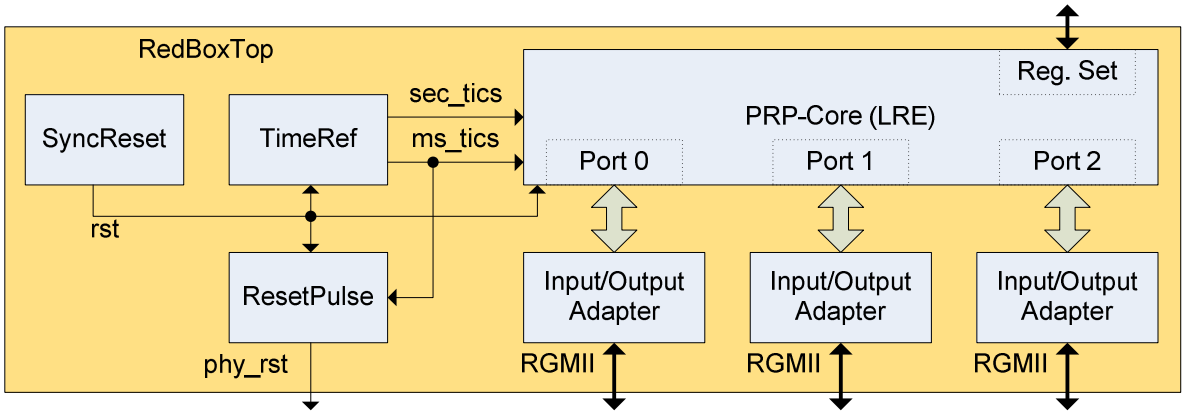


Figure 10: RedBoxTop block diagram

Signal	Value	Description
g_PHY_RST_MS	10	Duration of PHY reset pulse at phy_rst output in ms. Consult PHY data sheet to set proper value.
g_MDC_FREQ_MHZ	1	Frequency of internally generated MDC clock (PHY_MDC) in MHz which is used to read the PHY register. Consult PHY data sheet to set proper value.
g_RSC_FREQ_MHZ	50	Register set clock (rs_clk) frequency in MHz. Any value between 20 and 125 MHz is allowed.
g_REF_FREQ_MHZ	250	Core clock (clk) frequency in MHz. Fixed to 250 MHz for current implementation.

Table 2: RedBoxTop interface generics description

Signal	Dir.	Width	Description
Infrastructure			
clk	In	1	250 MHz core clock input
arst	In	1	Asynchronous reset
Register Set interface			
rs_clk	In	1	50 MHz Register Set clock input
rs_arst	In	1	Asynchronous reset
rs_irq	Out	1	Interrupt request line to external µCU
rs_rd_en	In	1	Register read enable
rs_wr_en	In	1	Register write enable
rs_addr	In	8	Register address
rs_rd_data	Out	32	Register read data
rs_wr_data	In	32	Register write data
SMI interface			
PHY_MDC	Out	1	MDC line connected to PHY
PHY_MDIO_I	In	1	Data input from top-level tristate-buffer connected to MDIO line of an external PHY
PHY_MDIO_O	Out	1	Data output to top-level tristate-buffer connected to MDIO line of an external PHY
PHY_MDIO_T	Out	1	Direction control of top-level tristate-buffer connected to MDIO line of external PHY
EXT_MDC	In	1	MDC line connected to an external µCU
EXT_MDIO_I	In	1	Data input from top-level tristate-buffer connected to MDIO line of an external µCU
EXT_MDIO_O	Out	1	Data output to top-level tristate-buffer connected to MDIO line of an external µCU
EXT_MDIO_T	Out	1	Direction control of top-level tristate-buffer connected to MDIO line of an external µCU
RGMII interface			
phy_rst	Out	1	PHY reset pulse output
rgmii_rx_array	In	3	RGMII input array to Input Adapter
rgmii_tx_array	Out	3	RGMII output array to Output Adapter

Table 3: RedBoxTop interface description

The Register Set interface style is similar to Altera Avalon bus. Therefore, Altera NIOS II µCU can be easily connected to the RedBox component. The Register Set interface is optional; if not used, drive *rs_rst* input with '1', all other inputs with '0' and leave *rs_rd_data* unconnected. In such a case, the preset register values are used.

Note: Free available RedBoxTop netlist expects 50 MHz Register Set clock at the *rs_clk* input. This limitation doesn't apply to commercially available PRP-Core, which accepts any clock between 20 MHz and 125 MHz.

During a write access to the Register Set, the data is latched every clock cycle. Hence, to avoid unintentional register value transitions, both register address and write data must be assigned in the same clock cycle as write enable is asserted and kept constant till write enable is de-asserted (Figure 11). The duration of a write cycle is not limited.

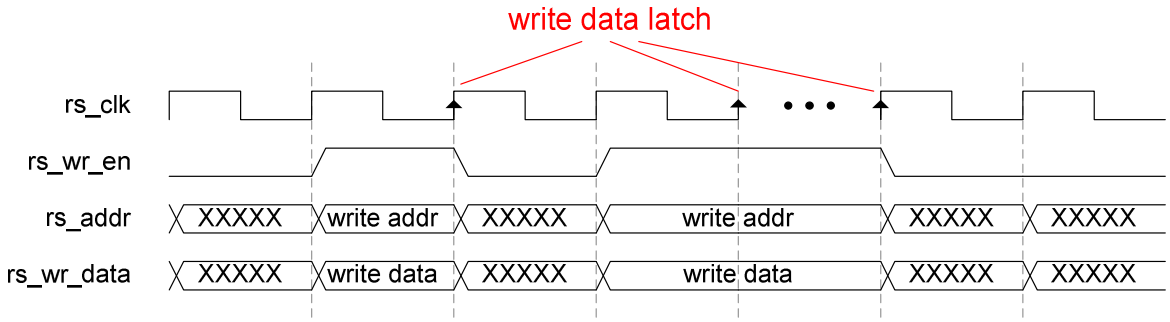


Figure 11: Register Set write cycle timing

During a register read access the selected register content is latched once to read data output (Figure 12). The read data output is then kept unchanged till a new read access is started.

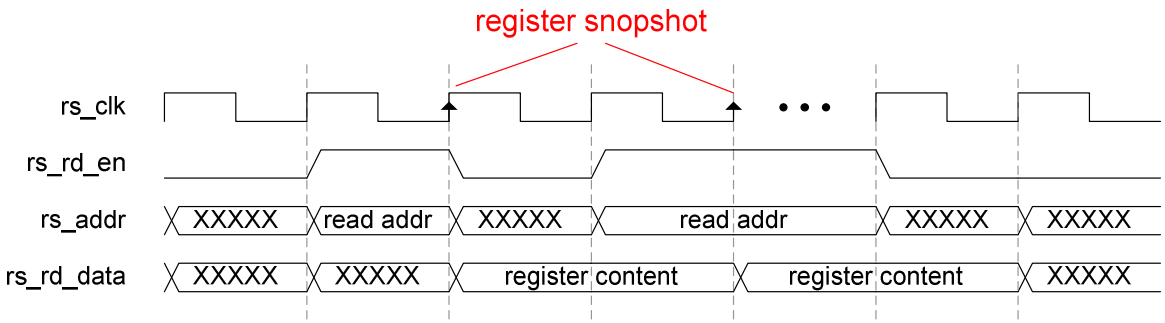


Figure 12: Register Set read cycle timing

2 Hardware design considerations

2.1 Serial Management Interface

The Serial Management Interface (SMI) is a serial bus, which is used to configure the register settings and to readout the status of the PHY devices. The PRP-Core uses the SMI bus to read periodically the Mode Status Registers of all PHYs and to update the link status in the LSTAT register with the retrieved information. However, the user can stop the PRP-Core from polling the PHY devices via SMI bus by setting Release SMI (RELS) bit in the LSTAT register. Once set and acknowledged by SMI Idle flag (SIDLE), user can access the SMI bus through EXT_MDIO and EXT_MDC interface signals of the PRP-Core. The PRP-Core enables then the bypass logic to the PHY_MDIO and PHY_MDC signals connected to the PHYs.

Note: The PHY devices should be connected to the same physical SMI bus and configured with different bus addresses. These addresses must be also set in the LSTAT register of the PRP-Core for proper SMI access.

2.2 RGMII timing closure

Generally, a RGMII transmitter generates the data signals (TXD) and control signal (TX_CTL) aligned to the transmit clock (TXC). However, at the RGMII receiver the receive clock (RXC) must appear delayed by 2 ns relative to the receive data (RXD, RX_CTL) change in order to guarantee setup and hold times of the flip-flops (Figure 13, Figure 14).

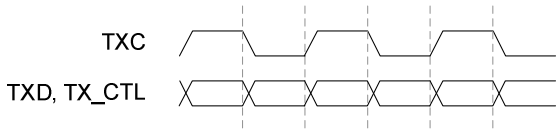


Figure 13: RGMII timing at the transmitter

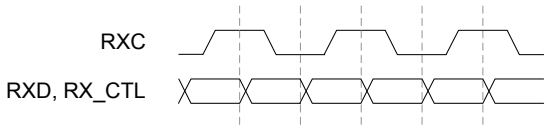


Figure 14: RGMII timing at the receiver

The receive clock delay can be introduced at the transmitter side (Figure 15, T_1), by appropriate PCB delay line (T_2) or at the receiver side (T_3).

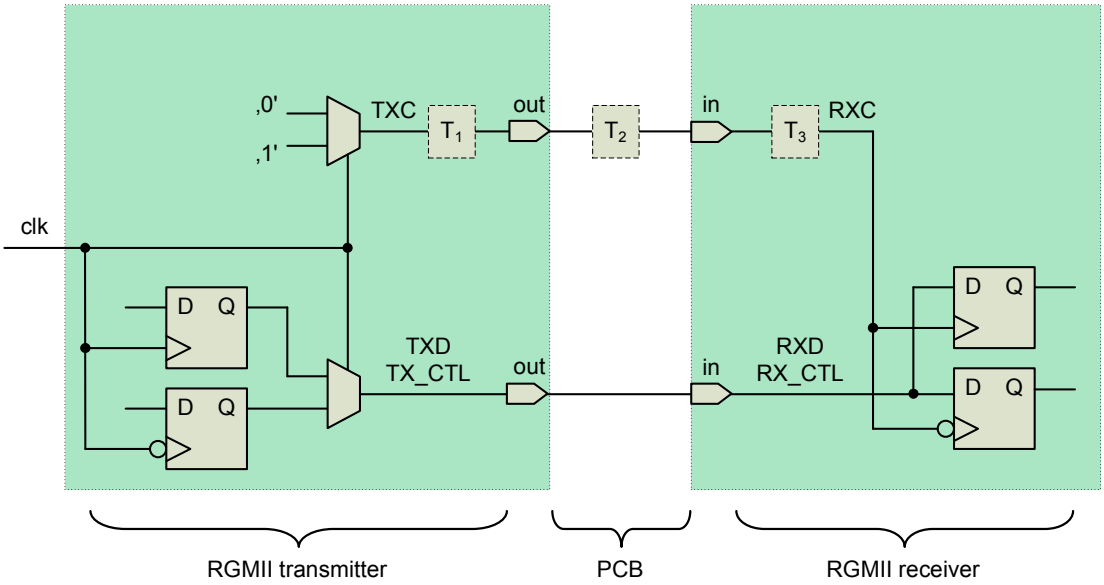


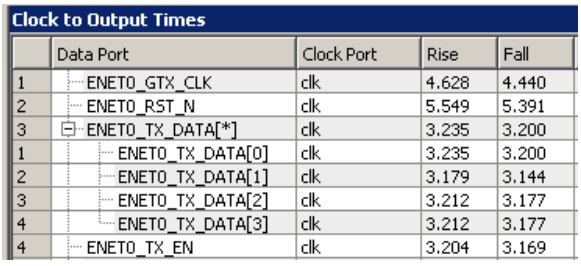
Figure 15: RGMII signal path diagram

The most PHY devices can be configured via SMI to introduce input or/and output delay. This however, requires a µCU, which can configure the PHY with proper settings after power-up via SMI. In general, PHY device is fully functional after power-up if the PHY bootstrap pins are hard-wired appropriately. Thus, in some use cases (e.g. Figure 7) SMI access is not available or even not desired. Therefore, methods to introduce inherent clock delay at the FPGA are shown in the Table 4.

FPGA function	Clock delay method	Notes
RGMII transmitter	Place the TXD and TX_CTL structures into IO-cells. Prevent placement of TXC structure into IO-cell.	The clock-to-output delay of registers inside the FPGA logic fabric is inherently higher than of those in IO-cells.
	Enable dedicated IO-cell output delay for the TXC output.	Most FPGA families provide configurable IO-cell output delay.
	Reduce drive strength and/or rise time of the TXC output.	Due to capacity of the TXC PCB line, the TXC level change is detected later at the receiver.
RGMII receiver	Use PLL for each TXC to introduce clock delay.	Not preferable due to limited PLL resources.
	Invert TXC input.	Inverting TXC input is equal to introducing 4 ns input delay.
	Enable dedicated IO-cell input delay for the TXD and TX_CTL inputs in conjunction with inverting TXC input.	Some FPGA families provide configurable IO-cell input delay.

Table 4: RGMII timing adjustment methods in the FPGA

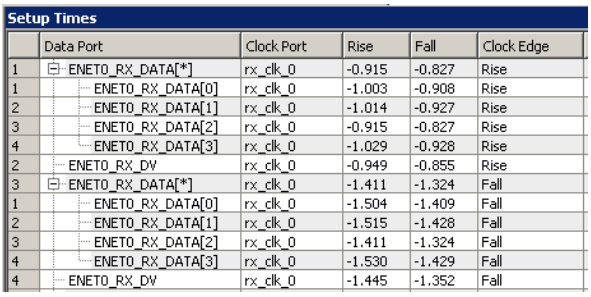
Independent of the method used to delay TXC, the FPGA designer is expected to create appropriate timing constraints and inspect the results of the FPGA design timing analysis (Figure 16, Figure 17).



Clock to Output Times

	Data Port	Clock Port	Rise	Fall
1	ENET0_GTX_CLK	clk	4.628	4.440
2	ENET0_RST_N	clk	5.549	5.391
3	ENET0_TX_DATA[*]	clk	3.235	3.200
1	ENET0_TX_DATA[0]	clk	3.235	3.200
2	ENET0_TX_DATA[1]	clk	3.179	3.144
3	ENET0_TX_DATA[2]	clk	3.212	3.177
4	ENET0_TX_DATA[3]	clk	3.212	3.177
4	ENET0_TX_EN	clk	3.204	3.169

Figure 16: RGMII timing analysis results at transmitter side (clock delay ~ 1.4 ns)



Setup Times

	Data Port	Clock Port	Rise	Fall	Clock Edge
1	ENET0_RX_DATA[*]	rx_clk_0	-0.915	-0.827	Rise
1	ENET0_RX_DATA[0]	rx_clk_0	-1.003	-0.908	Rise
2	ENET0_RX_DATA[1]	rx_clk_0	-1.014	-0.927	Rise
3	ENET0_RX_DATA[2]	rx_clk_0	-0.915	-0.827	Rise
4	ENET0_RX_DATA[3]	rx_clk_0	-1.029	-0.928	Rise
2	ENET0_RX_DV	rx_clk_0	-0.949	-0.855	Rise
3	ENET0_RX_DATA[*]	rx_clk_0	-1.411	-1.324	Fall
1	ENET0_RX_DATA[0]	rx_clk_0	-1.504	-1.409	Fall
2	ENET0_RX_DATA[1]	rx_clk_0	-1.515	-1.428	Fall
3	ENET0_RX_DATA[2]	rx_clk_0	-1.411	-1.324	Fall
4	ENET0_RX_DATA[3]	rx_clk_0	-1.530	-1.429	Fall
4	ENET0_RX_DV	rx_clk_0	-1.445	-1.352	Fall

Figure 17: RGMII timing analysis results at receiver side (clock delay ~ 0.9-1.4 ns)

2.3 FPGA pinout

Due to high-speed Double Data Rate (DDR) communication with the PHY the proper FPGA pin selection for RGMII interface is a very critical part of hardware design. Following rules should be obeyed during the FPGA IO pin selection process:

- Use dedicated clock inputs for RXC and reference clock input signals.
- If 250 MHz core clock is generated via a PLL, ensure that dedicated clock routing resources are used for reference clock input to the PLL cell.
- Don't use dedicated clock inputs for RX_CTL and RXD inputs. In general, such inputs don't have IO-cell registers and have a different input delay when compared to general IOs.
- Don't use FPGA IOs with dedicated function used during configuration.
- Use pins with same clock-to-output delay (t_{co}) for the same port RGMII transmit signals (TXC, TX_CTL and TXD). **Note:** At some FPGA families the t_{co} differs between top/bottom and left/right IO banks.

2.4 FPGA resource usage and device selection

Due to high customization grade of the PRP-Core only resource usage of a few meaningful configurations is given (Table 5). Resource usage of a specific core configuration can be provided on request.

Config Nr.	Output Adapter FIFO size		Port A/B Receive FIFO	Tagger FIFO size	Entry Table size	Nodes Table
	Port A/B	Port C				
1	1 kByte	8 kByte	4 kByte	2 kByte	512	no
2	1 kByte	8 kByte	4 kByte	2 kByte	512	yes
3	1 kByte	32 kByte	4 kByte	2 kByte	4096	yes

Table 5: Sample core configuration details

As easily can be seen, neither the FIFO nor the Duplicate Table sizes have a noteworthy impact on logic resource usage except M9K RAM block count (Table 6). As shown by the timing results, the device speed grade -7 is sufficient for any PRP-Core configuration if Altera Cyclone IV devices are used.

Config Nr.	LEs	4-input LUTs	REGs	M9K blocks	Max. clock
1	~7300	~5000	~5400	34	272 MHz
2	~9000	~6300	~6600	42	277 MHz
3	~9100	~6300	~6700	102	257 MHz

Table 6: PRP-Core resource usage for the Altera Cyclone IV target technology (max. core clock is given for FPGA speed grade '-I7')

3 Register Set

3.1 Summary

The Register Set summary in the Table 7 provides a quick reference to the register addresses, names, reset values and short descriptions. The address range is divided in three logical groups. The first register group up to the address 0x0F is reserved for general core control and status registers. The address range from 0x10 to 0x18 is reserved to read-only Monitoring Data Set and other event counters. The last address range from 0x20 to 0x26 is reserved for the Nodes Table readout registers.

Address	Register	Reset	Description
0x00	CVER	0x0800_0101	Core Version Register
0x01	CCTRL1	0x6000_1190	Core Control Register #1
0x02	CCTRL2	0xC000_3C00	Core Control Register #2
0x03	CCTRL3	0x0012_3456	Core Control Register #3
0x04	CCTRL4	0x0000_7890	Core Control Register #4
0x08	CSTAT[1]	0x0000_0000	Core Status Register
0x0B	LSTAT[1]	0x0000_8080	Link Status Register
0x0C	IER	0x0000_0000	Interrupt Enable Register
0x0D	ISR	0x0000_0000	Interrupt Status Register
0x0F	FESTAT	0x0000	FIFO Error Status Register
0x10	MISMA[1]	0x0000_0000	Path Mismatch Counter port A
0x11	MISMB[1]	0x0000_0000	Path Mismatch Counter port B
0x12	RXFMA[1]	0x0000_0000	Received Frame Counter port A
0x13	RXFMB[1]	0x0000_0000	Received Frame Counter port B
0x14	RXFMC	0x0000_0000	Received Frame Counter port C
0x15	ERFMA[1]	0x0000_0000	Erroneous Frame Counter port A
0x16	ERFMB[1]	0x0000_0000	Erroneous Frame Counter port B
0x17	ERFMC	0x0000_0000	Erroneous Frame Counter port C
0x18	FMDP	0x0000_0000	FIFO Frame Drop Counters
0x20	NSTAT[2]	-	Node Status Register
0x21	NMAC0[2]	-	Node MAC0..3 Register
0x22	NMAC4[2]	-	Node MAC4..5 Register
0x23	NRXA[2]	-	Node Receive LAN A Counter
0x24	NRXB[2]	-	Node Receive LAN B Counter
0x25	NERRA[2]	-	Node Error LAN A Counter
0x26	NERRB[2]	-	Node Error LAN B Counter

Table 7: Register set summary

[1]**Note:** Register which contain Monitoring Data Set defined in IEC 62439-3.4:2011

[2]**Note:** Register which contain Nodes Table attributes defined in IEC 62439-3.4:2011

3.2 Description

3.2.1 Conventions

A register bit mapping description consists of three rows (e.g. Table 8) with appended bit field descriptions. The first row identifies bits positions occupied by a bit field. The registers are always 32 bit width. However, not always all register bits are used. Thus, the second row shows widths and names of the used fields. If some bit positions are not used, then they are marked as “reserved”. The content of the reserved bit positions should be ignored (i.e. masked out) when read access is done and always zeroed for a write access. The third row provides supported access modes of a register field:

- Read only (ro),
- Read/write (rw),
- Write only (wo),
- Read/clear (rc) – after the read access the value of the field is cleared.
- Write/clear (wc) – after the write access the value of the field is cleared.

The third row also shows the value of a register field after a reset. If the reset value is not defined, it is shown by “x” (don’t care) character.

3.2.2 Core Version Register

The Core Version Register provides PRP-Core version and subversion information. Furthermore it provides the details of the supported feature set (e.g. Nodes Table).

31 28	27	26 16	15 8	7 0
CID	NTAB	reserved	VER	SUBV
ro - 0x0	ro – 0/1	-	ro - 0x01	ro - 0x01

Field	Description
CID	Core ID. Used to differentiate between the available redundancy IP cores.
NTAB	Nodes Table. If set, the PRP-Core contains the Nodes Table, which is an optional core feature.
VER	Core Version. Incremented on major (e.g. architectural) upgrades.
SUBV	Core Subversion. Incremented on minor changes and/or bug fixes.

Table 8: Core Version Register (CVER, 0x00)

3.2.3 Core Control Register

The Core Control register contain fields to control the PRP-Core behavior.

31	30	29	28	27 16	15 10	9 0
CRST	UTAG	TAG	VFEN	VID	MFGT	EFGT
wc - 0	rw - 1	rw - 1	rw - 0	rw - 0x000	rw - 0x04	rw - 0x190

Field	Description
CRST	Core Reset. If set, then the PRP-Core is resetted. This bit is automatically cleared.
UTAG	Untag. If set, then frames received from PRP network with detected RCT and correct LAN ID field are untagged before passing them to non-redundant network. Avoid using this setting if SANs are connected to the PRP network directly. Otherwise there is a risk of untagging and thus corrupting frames received from SANs when their last 6 bytes of payload unintentionally represent a well-formed RCT with correct LDSU field.
TAG	If set, then all outgoing frames are tagged. If cleared, then the frames received from non-redundant network are passed to PRP network unchanged. The Supervision frames are however still tagged.
VFEN	VLAN Filtering Enable. If set, then VLAN ID-based frame filtering is done and generated Supervision frames are VLAN-tagged with VLAN ID stored in VID field.
VID	VLAN Identifier (ID). If the VFEN field is set, then additional frame filtering is done based on this ID. All incoming VLAN-tagged frames with different VLAN ID are discarded and not passed to non-redundant network. Furthermore this ID is used for VLAN tagging of Supervision frames.
MFGT	MAC Forget Time in minutes. A MAC entry is removed from MAC Table after this time if the entry wasn't refreshed by the MAC learning process.
EFGT	Entry Forget Time in ms. A frame entry is held during this of period time in the Entry Table. After elapsing of this time period, the entry is cleared (aged out). The standard defines a setting of 400 ms for 100 MBit networks. In the GBit networks the user is advised to use 40 ms instead.

Table 9: Core Control Register #1 (CCTRL1, 0x01)

31	30	29	28	27	26 16	15 8	7 0
SPV	DPR	NREQ	RBS	FWSV	reserved	NFGT	SBMAC5
rw - 1	rw - 1	rw – 0	rw – 0	rw – 0	-	rw - 0x3C	rw - 0x00

Field	Description
SPV	Supervision frame. If set, then Supervision frames are generated for each node connected to non-redundant network and passed to PRP network. **Note:** Supervision frames are always tagged with a RCT.
DPR	Duplicate Reject. If set, then duplicates received from the PRP network are dropped (duplicate reject mode). If cleared, then all frames are passed unchanged (with RCT) from PRP network to non-redundant network and visa-versa (duplicate accept mode). **Note:** The duplicate accept mode can lead to receive path FIFOs overflow conditions causing undesired frame drops. Thus this feature should be used for debugging during PRP network installation only.
NREQ	Nodes Table Read Request. If set, then next valid entry is searched in the Nodes Table and stored in the registers at 0x20-0x26 address range. This bit is automatically cleared after processing of the read request. A clearing event of this bit is an interrupt source. **Note:** Avoid polling of the NREQ bit, use interrupt functionality instead.
RBS	RedBox Supervision mode. If set, the generated Supervision frames contain TLV2 and RedBoxMacAddress fields. This bit should be set if the PRP-Core is used as a RedBox. The RedBoxMacAddress is set via CCTRL3 and CCTRL4 registers.
FWSV	Forward Supervision frames. If set, Supervision frames are passed from PRP network to non-redundant network. In general, there is no need to forward the frames to non-redundant network hence the supervision frames are generated and fully processed inside the PRP-Core. **Note:** The duplicate reject and untag settings (DPR and UTAG bits) are also applicable to supervision frames passed to non-redundant network.
NFGT	Node Forget Time in minutes. An entry is removed from Nodes Table if no frames were received from the according node for the time specified in this field. This value is also used for SANA/B-moving detection algorithm.
SBMAC5	Supervision Broadcast MAC byte #5. By default the broadcast MAC of the Supervision frames is 01-15-4E-00-01-**XX**. The **XX** value is specified by SBMAC5 field. By default it is 0x00. However if a conflict arises, the value can be changed between 0x00 and 0xFF.

Table 10: Core Control Register #2 (CCTRL2, 0x02)

31 24	23 16	15 8	7 0
RBMAC0	RBMAC1	RBMAC2	RBMAC3
rw - 0x00	rw - 0x12	rw - 0x34	rw - 0x56

Field	Description
RBMAC0...3	RedBoxMacAddress bytes 0..3. The RedBoxMacAddress field is specified by the standard and is used for Supervision frame generation when the PRP-Core is running in RedBox Supervision mode (RBS bit is set). The user is responsible to overwrite the reset values with proper contents. The SPV bit must be cleared when the contents of the CCTRL3 and CCTRL4 register are modified.

Table 11: Core Control Register #3 (CCTRL3, 0x03)

31 16	15 8	7 0
reserved	RBMAC4	RBMAC5
-	rw - 0x78	rw - 0x90

Field	Description
RBMAC4...5	RedBoxMacAddress bytes 4..5. See CCTRL3 register description for details.

Table 12: Core Control Register #4 (CCTRL4, 0x04)

3.2.4 Core Status Register

The Core Status Register provides read-only information of current PRP-Core status. The field SendSeq is a mandatory part of standard-defined Monitoring Data Set.

31	30 16	15 0
NFULL	reserved	SendSeq
ro - 0	-	ro - 0x0000

Field	Description
NFULL	Nodes Table Full. If set, then no free slot was found in the Nodes Table to create a new node entry. This bit is sticky and is an interrupt source.
SendSeq	Sequence Number. Represents the sequence number which will be used to tag next outgoing duplicates. The sequence number is incremented with every duplicate pair tagged and sent to PRP network.

Table 13: Core Status Register (CSTAT, 0x08)

3.2.5 Link Status Register

This register provides read-only information of link status of the Port A/B/C PHYs. Prior readout and processing of link status information the PHY address fields should be initialized to the appropriate values.

31	30	29 21	20 19	18 14	13 12	11 7	6 5	4 0
RELS	SIDLE	reserved	LSC	PHYC_ADR	LSB	PHYB_ADR	LSA	PHYA_ADR
rw - 0	ro - 0	-	ro - 0	rw - 0x02	ro - 0	rw - 0x01	ro - 0	rw - 0x00

Field	Description
RELS	Release SMI. If set, any SMI access to the PHY registers will be finished and the control over the SMI bus will be passed to the external SMI controller. This will be signaled by SIDLE bit set.
SIDLE	SMI Idle. Set, if the control over the SMI bus is passed to the external SMI controller. In this case the link status information stored in the PHY registers is no longer monitored.
LSA/B/C	Link Status port A/B/C. Link status and link speed information of all three RGMII ports. The detection of the link status is done by the according Input Adapter and the SMI Controller. Thus, the PHY addresses in the fields PHY0/1/2_ADR should be set to appropriate values. The links status changing is an interrupt source.
PHYA/B/C_ADR	PHY Port A/B/C addresses. These fields define addresses of the PHYs attached to the SMI bus and should be initialized for proper link status detection shown in LSA/B/C fields. The correspondence of the PHYs, ports and networks is:

LSA/B/C	Link status
“00”	No link
“01”	10Mbit
“10”	100Mbit
“11”	1000Mbit

PHY/Port	Network
A/0	LAN A
B/1	LAN B
C/2	non-redundant

Table 14: Link Status Register (LSTAT, 0x0B)

3.2.6 Interrupt Enable and Status Registers

The Interrupt Enable Register is used to enable interrupt sources. The interrupt sources are only evaluated, if according interrupt enable bit is set. Clearing of an interrupt enable bit has no impact to interrupt bits already set in Interrupt Status Register.

31 … 5	4	3	2	1	0
reserved	FDIE	NRIE	FEIE	NFIE	LSIE
-	rw - 0	rw - 0	rw - 0	rw - 0	rw - 0

Field	Description
FDIE	Frame Drop Interrupt Enable.
NRIE	Nodes Table Read Request Interrupt Enable.
FEIE	FIFO Error Interrupt Enable.
NFIE	Nodes Table Full Interrupt Enable.
LSIE	Link Status Interrupt Enable.

Table 15: Interrupt Enable Register (IER, 0x0C)

A bit in the Interrupt Status Register (ISR) is set, only if the interrupt condition is fulfilled and the according interrupts enable bit in IER register is set. The interrupt line to the µCU is asserted, if the ISR register is non-zero. The only way to release the interrupt line, is to read the ISR register and thus to clear all interrupt status bits.

31 … 5	4	3	2	1	0
reserved	FDIS	NRIS	FEIS	NFIS	LSIS
-	rc - 0	rc - 0	rc - 0	rc - 0	rc - 0

Field	Description
FDIS	Frame Drop Interrupt Status. Is set when a frame was dropped either in the transmit or receive direction and thus TXFMDP or RXFMDP Counter was incremented.
NRIS	Nodes Table Read Request Interrupt Status. Is set when the read request to the Nodes Table has been processed and thus the NREQ bit was cleared.
FEIS	FIFO Error Interrupt Status. Is set if the FESTAT register is non-zero.
NFIS	Nodes Table Full Interrupt Status. Is set if the NFULL bit is set.
LSIS	Link Status Interrupt Status. Is set if any of the link status fields (LSA/B/C) in CSTAT register has been changed.

Table 16: Interrupt Status Register (ISR, 0x0D)

3.2.7 FIFO Error Status Register

The FIFO Error Status register provides information on erroneous FIFO over- and underflow states. Such non-recoverable FIFO states are avoided in the PRP-Core by design, thus the user should never experience a non-zero value in this register. However if a non-zero value is read from the FESTAT register, then the PRP-Core has experienced a non-recoverable malfunction and should be reset via Core Control Register to avoid enduring data losses. Furthermore, the user is kindly requested to provide the value read to the IP owner for debugging purposes.

31 … 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved	TXOC	TXOB	TXOA	TXUC	TXUB	TXUA	RXFUB	RXFUA	RXAOB	RXAOA	RXAUB	RXAUA	TXFU	TXAO	TXAU
-	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0	ro - 0

Field	Description
RXnn	FIFO Error Status in receive path. If not zero, reset the PRP-Core. These bits are sticky and are an interrupt source.
TXnn	FIFO Error Status in transmit path. If not zero, reset the PRP-Core. These bits are sticky and are an interrupt source.

Table 17: FIFO Error Status Register (FESTAT, 0x0F)

3.2.8 Monitoring Data Set Registers

Both Frame Path Mismatch Counters (MISMA/B) count the tagged frames, which LAN ID field in the RCT mismatches the physical receive path (port 0/1 for LAN A/B). Both counters are an optional part of standard-defined Monitoring Data Set.

31 … 0
CntErrWrongLanA/B
ro – 0x00000000

Field	Description
CntErrWrongLanA/B	Count of tagged frames received from PRP network with wrong LAN ID at the ports A and B.

Table 18: Frame Path Mismatch Counters (MISMA/B, 0x10/11)

The Received Frame Counters (RXFMA/B/C) count the number of frames received at the according port. The counters of the ports A and B are an optional part of standard-defined Monitoring Data Set.

31 … 0
CntReceivedA/B/C
ro – 0x00000000

Field	Description
CntReceivedA/B/C	Count of frames received at ports A/B/C.

Table 19: Received Frame Counters (RXFMA/B/C, 0x12/13/14)

The Erroneous Frame Counters (ERFMA/B/C) count the number of frames with wrong FCS received at the according port. The counters of the ports A and B are an optional part of standard-defined Monitoring Data Set.

31	0
CntErrorA/B/C	
ro - 0x00000000	

Field	Description
CntReceivedA/B/C	Count of frames with wrong FCS received at ports A/B/C.

Table 20: Erroneous Frames Counters (ERFMA/B/C, 0x15/16/17)

The Frame Drop Counters (FMDP) provide information, how many frames were dropped due to lack of memory in either receive (RXFMDP) or transmit (TXFMDP) FIFOs. Such frame drops happen in a well-controlled manner and can be an indication of under-estimated FIFO size requirements.

In the receive path the frame drops can never be fully eliminated by increasing FIFO size if SANs are present in the PRP network. The worst-case scenario is when two SANs in different sub-networks are sending data to a DAN at the same time with full link speed. Then the receive FIFOs overflow is unavoidable, because the data traffic from both ports A and B is merged by the RPR-Core to a single output port, overcrowding it rapidly. Thus, removing SANs from a PRP network is a proper way to avoid the frame drops in the receive path.

In the transmit path the Tagger adds 6 bytes long PRP RCT to each outgoing frame, increasing transmit bandwidth requirement of the ports A and B potentially above the link speed. This condition is however extremely unlikely and is handled properly with moderate Tagger FIFO size increase.

31	16	15	0
TXFMDP		RXFMDP	
ro - 0x0000		ro - 0x0000	

Field	Description
RXFMDP	Count of the frames dropped in the receive path.
TXFMDP	Count of the frames dropped in the transmit path.

Table 21: Frame Drop Counters (FMDP, 0x18)

3.2.9 Node Entry Registers

The Node Entry Registers represent the interface to the optional Nodes Table. After finishing the readout of the next valid Nodes Table entry (see also CCTRL2 register description), the entry attributes are accessible via the Node Entry Registers. Only attributes of a single node entry are accessible after a Nodes Table readout. To read the next valid node entry from Nodes Table another readout should be initiated.

The Node Status Register provides general node status information. The fields SanA/B and TimeLastSeenA/B are part of standard-defined Nodes Table attributes.

31	30	29	28	27	26 24	23 16	15 8	7 0
EVAL	DACC	DREJ	SANB	SANA	reserved	EADR	TimeLastSeenB	TimeLastSeenA

ro - 0	ro - x	ro - x	ro - x	ro - x	-	ro - x	ro - x	ro - x

Field	Description
EVAL	Entry Valid. If set, then the node entry read from the Nodes Table is valid. If cleared, then the Nodes Table contains no valid entries. This is only the case if this DAN is isolated from the rest of the PRP network or it's the only node in the PRP network.
DACC	Duplicate Accept. Set after reception of a Supervision frame with TLV1.Type field set to 0x21 value, which signals that the according DAN accepts duplicates.
DREJ	Duplicate Reject. Set after reception of a Supervision frame with TLV1.Type field set to 0x20 value, which signals that the according DAN rejects duplicates.
SanA/B	Single Attached Node LAN A/B. This bit signals the visibility of the node at LAN A/B sub-networks of a PRP network. In conjunction with DACC and DREJ bits it can be used to identify SANs, DANs and disconnected DAN ports: **SANB** | **SANA** | **DACC or DREJ** | **Interpretation** 0 | 1 | 0 | SANA 1 | 0 | 0 | SANB 0 | 1 | 1 | DAN disconnected from LAN B[1] 1 | 0 | 1 | DAN disconnected from LAN A[1] 1 | 1 | 1 | DAN [1]**Note:** Only DANs send Supervision frames. [1]**Note:** If all DANs are only visible through LAN A resp. LAN B, then **this** node is most probably disconnected from the LAN B resp. LAN A sub-network.
TimeLastSeenA/B	Time in seconds since the last frame reception through LAN A/B from the according node. If the TimeLastSeenA respective TimeLastSeenB reaches NFGT value set in CCTRL2 register, then SANA respective SANB flag is cleared. If both SANA/B flags were cleared, then the Node Entry is removed from the Nodes Table, since the node is no longer visible in the PRP network. **Note:** Since the PRP-Core doesn't support time synchronization and thus local time reference, the meaning of the TimeLastSeenA/B fields deviates from standard specification.
EADR	Nodes Table Entry Address. The address at which the node entry is stored in the Nodes Table. Once a node entry is created, its attributes are stored at this address in the Nodes Table as long as the according node is visible in the PRP network.

Table 22: Node Status Register (NSTAT, 0x20)

The Node MAC0..3 and MAC4..5 Node Entry registers contain the MAC address of the node. The MAC byte with the index 0 (MAC0) is received first during frame transmission (i.e. the complete MAC is MAC0:MAC1:MAC2:MAC3:MAC4:MAC5). The MAC0..MAC5 fields are part of standard-defined Nodes Table attributes.

Note: Either SMAC field of non-Supervision frames or MacAddress field of Supervision frames is used as MAC reference.

31 24	23 16	15 8	7 0
MAC0	MAC1	MAC2	MAC3
ro - x	ro - x	ro - x	ro - x

Field	Description
MAC0..3	MAC address bytes 0..3 of the node.

Table 23: Node MAC0..3 Register (NMAC0, 0x21)

31 16	15 8	7 0
reserved	MAC4	MAC5
-	ro - x	ro - x

Field	Description
MAC4..5	MAC address bytes 4..5 of the node.

Table 24: Node MAC4..5 Register (NMAC4, 0x22)

The Node Receive LAN A/B Counters count the frames received from the according node over LAN A respective LAN B. The fields CntReceivedA/B are part of standard-defined Nodes Table attributes.

31 0
CntReceivedA/B
ro - x

Field	Description
CntReceivedA/B	Number of frames received from the according node over LAN A/B

Table 25: Node Receive LAN A/B Counter (NRXA/B, 0x23/24)

The Node Error LAN A/B Counters count the frames received from the according node with wrong LAN identifiers. The fields CntErrWrongLanA/B are part of standard-defined Nodes Table attributes.

31 0
CntErrWrongLanA/B
ro - x

Field	Description
CntErrWrongLanA/B	Number of frames that were received from the according node with the wrong LAN identifier over LAN A respective LAN B.

Table 26: Node Error LAN A/B Counter (NERRA/B, 0x25/26)

4 Appendix

4.1 Document history

Version	Date	Author	Comment
1.01	2014-08-03	VM	Added FWSV bit definition to Register Set. Resource table usage update. Copyright notice update. Core version increased to 1.0.01
1.00	2014-05-17	VM	Initial version